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PATENT APPLICATION
Docket No. 11675.76.3

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND
INTERFERENCES

In re application of:		
	Gurtej Sandhu et al.	
		Art Unit
Serial No.:	09/627,649	2814
Filed:	July 28, 2000	
For:	INTERLEVEL DIELECTRIC STRUCTURE	
Confirmation No.:	2273	
Examiner:	Tuan Quach	

CERTIFICATE OF EXPRESS MAIL UNDER 37 C.F.R. § 1.10

I hereby certify that the following documents are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. § 1.10 in an envelope addressed to: Mail Stop Appeal Brief – Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the 7th day of June 2004.

- Appeal Brief of Appellant
- Credit Card Payment Form PTO-2038 for $330.00
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- Postcard

Respectfully submitted,

Gregory M. Taylor
Attorney for Appellants
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TRANSMITTAL OF APPEAL BRIEF UNDER 37 C.F.R. § 1.192

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith in triplicate is a Brief of Appellant for entry in the above-identified application. Appellant has filed a timely Notice of Appeal from the action of the Examiner dated October 6, 2003. Also enclosed are the following:

x A Certificate of Express Mail Under 37 C.F.R. § 1.10

x Credit Card Payment Form PTO-2038 authorizing payment of $330.00 for the filing fee.

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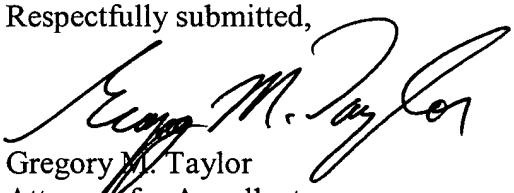
x The Commissioner is hereby authorized to charge payment of any patent application processing fees under 37 CFR 1.17 associated with this communication or credit any overpayment to Deposit Account No. 23-3178. Duplicate copies of this sheet are attached.

Dated this 7th day of June 2004.

Respectfully submitted,



Gregory M. Taylor
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Examiner:	Tuan Quach	)

BRIEF OF APPELLANT

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Appellants, Gurtej Sandhu et al., have filed a timely Notice of Appeal from the action of the Examiner in rejecting pending claims 6-18 in this application in the Office Action dated October 6, 2003. This brief is being filed under the provisions of 37 C.F.R. § 1.192. The filing fee of $330.00, as set forth in 37 C.F.R. § 1.17(c) is submitted herewith.

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REAL PARTY IN INTEREST

The real party in interest is Micron Technology, Inc., by way of assignment from Gurtej Sandhu, Anand Srinivasan, and Ravi Iyer, who are the named inventors in the present application. The assignment documents were recorded at Reel No. 8278, Frame 0650 in the United States Patent and Trademark Office on December 6, 1996.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

STATUS OF CLAIMS

Claims 6-18 are pending and appealed in the present application. Claims 1-5 have been cancelled.

STATUS OF AMENDMENTS

All amendments have been previously entered.

SUMMARY OF INVENTION

The present invention is directed to an interlevel dielectric structure comprising a single first dielectric layer 14 situated on a semiconductor substrate 12, with the single first dielectric layer 14 having an upper surface, and a plurality of lines of a two-layer conductive material extending along the upper surface of the single first dielectric layer 14. Each line of the plurality of lines has an upper surface, a lower surface, and at least one side surface. Adjacent lines of the plurality of lines have spaces situated therebetween. A first layer 40 of the two-layer

conductive material of the plurality of lines is in contact with the upper surface of the single first dielectric layer 14, and a second layer 42 of the two-layer conductive material of the plurality of lines comprises a refractory metal nitride. A single second dielectric layer 21 is above both the plurality of lines and the single first dielectric layer 14, with the single second dielectric layer 21 having a lower surface in contact with the upper surface of each line of the plurality of lines. A single dielectric material 17 is situated in the space between adjacent lines of the plurality of lines, with the single dielectric material 17 not extending over the upper surface of each line of the plurality of lines. An upper surface of the single dielectric material 17 is higher than the upper surface of each line of the plurality of lines, and a lower surface of the single dielectric material is lower than the lower surface of each line of the plurality of lines (*see* Figs. 8 and 9, Spec. pp. 13-14).

ISSUES

1. Whether claims 6-9 and 11-13 are unobvious over U.S. Patent No. 5,708,303 to Jeng (hereafter "*Jeng* '303") singly or with U.S. Patent No. 6,087,250 to Hyakutake (hereafter "*Hyakutake*").

2. Whether claims 14 and 16-18 are unobvious over *Jeng* '303 singly or with *Hyakutake.*

3. Whether claims 10 and 15 are unobvious over *Jeng* '303 singly or with *Hyakutake,* and further in view of U.S. Patent No. 5,486,493 to Jeng (hereafter "*Jeng* '493").

4. Whether claims 12 and 17 are unobvious over *Jeng* '303 singly or with *Hyakutake,* and further in view of U.S. Patent No. 5,420,075 to Homma et al. (hereafter "*Homma*").

5. Whether claims 6-18 should have been rejected under the judicially created doctrine of obviousness-type double patenting over U.S. Patent No. 6,107,686 in view of Jeng '303.

GROUPING OF CLAIMS

Claims 6-9, 11, and 13 stand or fall together. Claims 14, 16, and 18 stand or fall together. Claims 10 and 15 stand or fall together. Claims 12 and 17 stand or fall together.

ARGUMENT

1. Claims 6-9 and 11-13 are Unobvious Over *Jeng* '303 Singly or Taken With *Hyakutake*

Claims 6-9 and 11-13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Jeng* '303 singly or with *Hyakutake*. For the reasons that follow, Appellants respectfully submit that claims 6-9 and 11-13 are unobvious over the cited references.

The law is well settled that to "establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation ... to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations." Furthermore, the "teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." (citations omitted) M.P.E.P. §§ 2142, 2143, p. 2100-121, -122, 8th ed. (Aug. 2001).

Independent claim 6 recites a plurality of lines of a "two-layer conductive material" extending along the upper surface of the single first dielectric layer, with "a first layer of the two-layer conductive material" being in contact with the upper surface of the single first dielectric layer, and "a second layer of the two-layer conductive material" comprising a refractory metal nitride.

In contrast, *Jeng* '303 teaches a multi-layered metal line of a metal barrier layer 62, a metal layer 58, and a metal cap layer 60 (*see* col. 3, lines 18-20; Figs. 1, 18). *Jeng* '303 does not teach or suggest a structure wherein the conductive lines are a "two-layer" conductive material, as recited in present claim 6. In addition, there is no teaching or suggestion that the cited structure of *Hyakutake* could be used in the device of *Jeng* '303.

Thus, Appellants submit that claim 6 and dependent claims 7-9 and 11-13 would not have been obvious over *Jeng* '303 singly or taken with *Hyakutake*.

2. Claims 14 and 16-18 are Unobvious Over *Jeng* '303 Singly or Taken With *Hyakutake*

Claims 14 and 16-18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Jeng* '303 singly or with *Hyakutake*. For the reasons that follow, Appellants respectfully submit that claims 14 and 16-18 are unobvious over the cited references.

Independent claim 14 recites a plurality of lines of a "two-layer conductive material" extending along the upper surface of the first dielectric layer, with "a first layer of the two-layer conductive material" being in contact with the upper surface of the first dielectric layer, and "a second layer of the two-layer conductive material" comprising titanium nitride.

Jeng '303 does not teach or suggest a structure wherein the conductive lines are a "two-layer" conductive material, as recited in present claim 14. In addition, there is no teaching or suggestion that the cited structure of *Hyakutake* could be used in the device of *Jeng* '303.

Appellants therefore submit that claim 14 and dependent claims 16-18 would not have been obvious over *Jeng* '303 singly or taken with *Hyakutake*.

3. Claims 10 and 15 are Unobvious Over *Jeng* '303 Singly or Taken With *Hyakutake* and further in view of *Jeng* '493

Claims 10 and 15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Jeng* '303 singly or with *Hyakutake* and further in view of *Jeng* '493. For the reasons that follow, Appellants respectfully submit that claims 10 and 15 are unobvious over the cited references.

Claims 10 and 15 depend from claims 6 and 14, respectively, and thus include the limitations thereof. As discussed above, claims 6 and 14 would not have been obvious over *Jeng* '303 or *Hyakutake*. In addition, *Jeng* '493 does not overcome the deficiencies of *Jeng* '303 or *Hyakutake*. Thus, even if the cited references are combined as suggested by the Examiner, not all of the claim limitations are met.

Accordingly, Appellants submit that claims 10 and 15 would not have been obvious over *Jeng* '303 singly or taken with *Hyakutake* and further in view of *Jeng* '493.

4. Claims 12 and 17 are Unobvious Over *Jeng* '303 Singly or Taken With *Hyakutake* and further in view of *Homma*

Claims 12 and 17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Jeng* '303 singly or with *Hyakutake* and further in view of *Homma*. For the reasons that follow, Appellants respectfully submit that claims 12 and 17 are unobvious over the cited references.

Claims 12 and 17 depend from claims 6 and 14, respectively, and thus include the limitations thereof. As discussed above, claims 6 and 14 would not have been obvious over *Jeng* '303 or *Hyakutake*. In addition, *Homma* does not overcome the deficiencies of *Jeng* '303 or *Hyakutake*. Thus, even if the cited references are combined as suggested by the Examiner, not all of the claim limitations are met.

Accordingly, Appellants submit that claims 12 and 17 would not have been obvious over *Jeng* '303 singly or taken with *Hyakutake* and further in view of *Homma*.

5. Rejection Under the Judicially Created Doctrine of Double Patenting

Claims 6-18 have been rejected under the judicially created doctrine of obviousness-type double patenting over claims 1-9 of U.S. Patent No. 6,107,686 in view of Jeng '303.

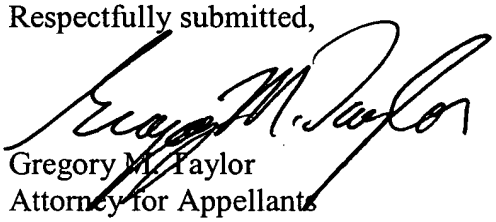
Appellants do not contest this rejection and are willing to file a terminal disclaimer to overcome the double patenting rejection of the claims once allowable subject matter is indicated.

CONCLUSION

In view of the foregoing, Appellants respectfully request the Board to overturn the Examiner's rejections of the appealed claims.

Dated this 7th day of June 2004.

Respectfully submitted,



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APPENDIX: CLAIMS ON APPEAL

6. An interlevel dielectric structure comprising:

a single first dielectric layer situated on a semiconductor substrate, said single first dielectric layer having an upper surface;

a plurality of lines of a two-layer conductive material extending along said upper surface of said single first dielectric layer; wherein:

each line of said plurality of lines has an upper surface, a lower surface, and at least one side surface;

adjacent lines of said plurality of lines have spaces situated therebetween;

a first layer of the two-layer conductive material of said plurality of lines is in contact with said upper surface of said single first dielectric layer; and

a second layer of the two-layer conductive material of said plurality of lines comprises a refractory metal nitride;

a single second dielectric layer above both said plurality of lines and said single first dielectric layer, said single second dielectric layer having a lower surface in contact with the upper surface of each line of said plurality of lines; and

a single dielectric material situated in said space between adjacent lines of said plurality of lines, said single dielectric material not extending over the upper surface of each line of said plurality of lines, an upper surface of said single dielectric material being higher than the upper surface of each line of said plurality of lines, and a lower surface of said single dielectric material being lower than the lower surface of each line of said plurality of lines.

7. The interlevel dielectric structure as defined in Claim 6, wherein:

said layer of refractory metal nitride has an electrical insulation spacer layer thereon, said electrical insulation spacer layer having thereon said single second dielectric layer; and

at least one side surface of the single dielectric material is in contact with at least one side surface of at least one of the plurality of lines.

8. The interlevel dielectric structure as defined in Claim 7, wherein said electrical insulation spacer layer is a silicon dioxide layer.

9. The interlevel dielectric structure as defined in Claim 6, wherein said refractory metal nitride is titanium nitride.

10. The interlevel dielectric structure as defined in Claim 6, wherein said single dielectric material comprises PTFE.

11. The interlevel dielectric structure as defined in Claim 6, wherein at least one of the single first dielectric layer and single second dielectric layer comprises silicon dioxide.

12. The interlevel dielectric structure as defined in Claim 6, wherein said conductive material of the first layer is selected from the group consisting of polysilicon, aluminum, copper, tungsten, and combinations thereof.

13. The interlevel dielectric structure as defined in Claim 6, wherein the single dielectric material has a dielectric constant of less than about 3.6.

14. An interlevel dielectric structure comprising:

a first dielectric layer situated on a semiconductor substrate, said first dielectric layer having an upper surface;

a plurality of lines of a two layer conductive material extending along said upper surface of said first dielectric layer; wherein:

each line of said plurality of lines has an upper surface, a lower surface, and at least one side surface;

adjacent lines of said plurality of lines have spaces situated therebetween;

a first layer of the two-layer conductive material of said plurality of lines is in contact with said upper surface of said first dielectric layer;

a second layer of the two-layer conductive material of said plurality of lines comprises a layer of titanium nitride;

said layer of titanium nitride has thereon a silicon dioxide spacer layer; and

said silicon dioxide spacer layer not being in contact with at least one side surface of at least one of the plurality of lines;

a second dielectric layer above both said plurality of lines and said first dielectric layer, said second dielectric layer having a lower surface in contact with the silicon dioxide spacer layer of each line of said plurality of lines; and

a dielectric material, having at least one side surface, situated in said space between adjacent lines of said plurality of lines, said dielectric material not extending over the upper surface of each line of said plurality of lines, an upper surface of said dielectric material being higher than the upper surface of each line of said plurality of lines, a lower surface of said dielectric material being lower than the lower surface of each line of said plurality of lines, and at least one side surface of the dielectric material being in contact with at least one side surface of at least one of the plurality of lines.

15. The interlevel dielectric structure as defined in Claim 14, wherein said dielectric material comprises PTFE.

16. The interlevel dielectric structure as defined in Claim 14, wherein at least one of the first and second dielectric layers comprises silicon dioxide.

17. The interlevel dielectric structure as defined in Claim 14, wherein said conductive material of the first layer is selected from the group consisting of polysilicon, aluminum, copper, tungsten, and combinations thereof.

18. The interlevel dielectric structure as defined in Claim 14, wherein the dielectric material has a dielectric constant of less than about 3.6.